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CyberWorkBench®
Pioneering C-based LSI Design

Practical Usage of "C-based Synthesis"

for Dynamic Reconfigurable Chips, and area reduction by performance balancing

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U can change.

Agenda

0) Our Chip Architecture – MPSoC (MxDHx)
1) Dynamic Reconfigurable Processor + C-synthesis
graphics, camcorder (embedded software)
2) Dedicated HW (ASIC) + C-synthesis
QoR for ASIP, Low Performance/High Performance HW
3) Summary

Other topics:
Design Flow: how we can integrate to my current flow?
legacy RTLs, RTL sim. assertion,
timing closure, ECO: can we do ?

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Preliminary: What is Behavior Synthesis?

Behavior in C

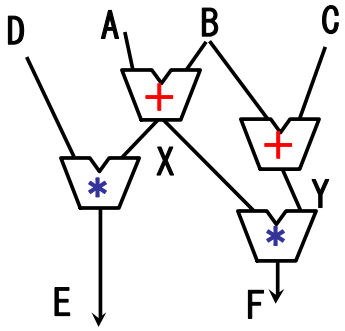
```
char A,B,C,D;
char E,F;
main(){
char X;
X = A + B;
E = X * D;
F = (B + C) * X;
}
```

8 Lines

Constraint 1

+ : 2
* : 2

Logic synthesis



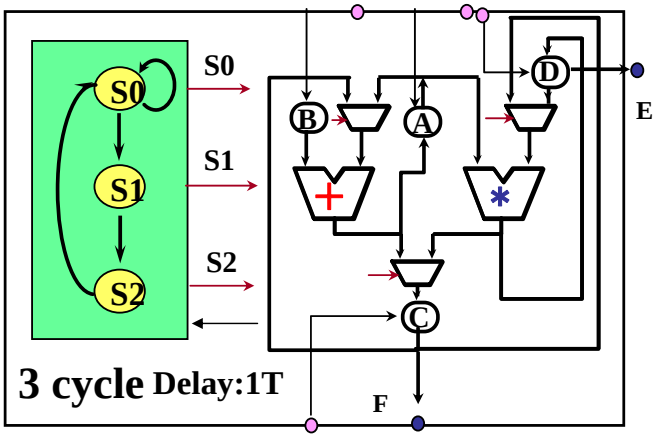
1cycle
Delay:2T

RTL

+ : 1
* : 1

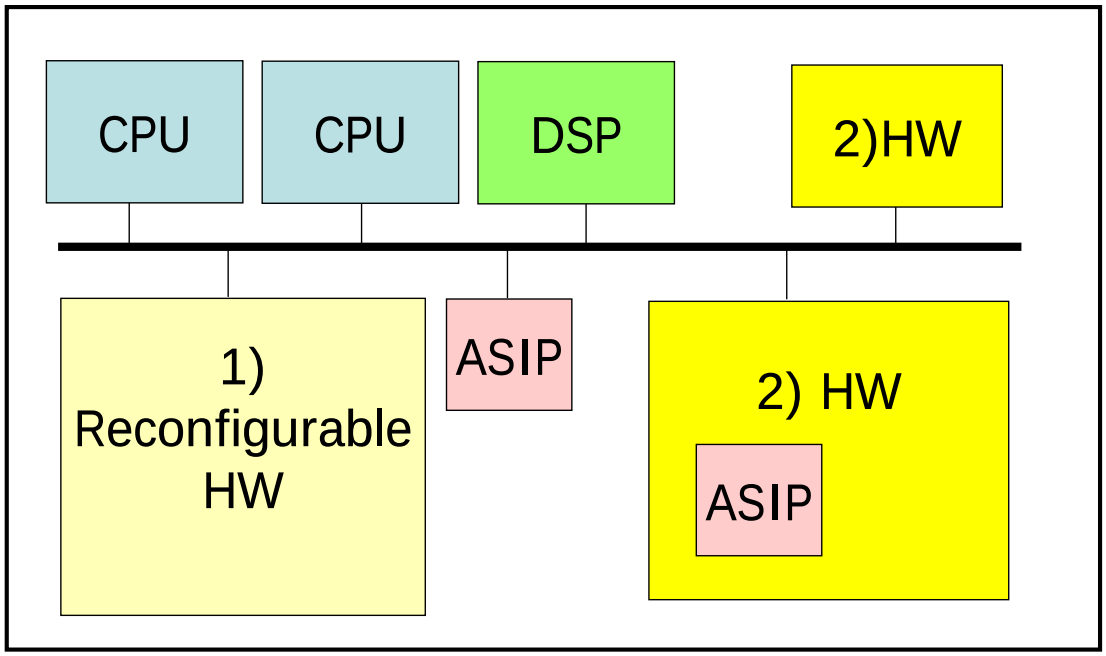
Constraint2

100 lines



3 cycle Delay:1T

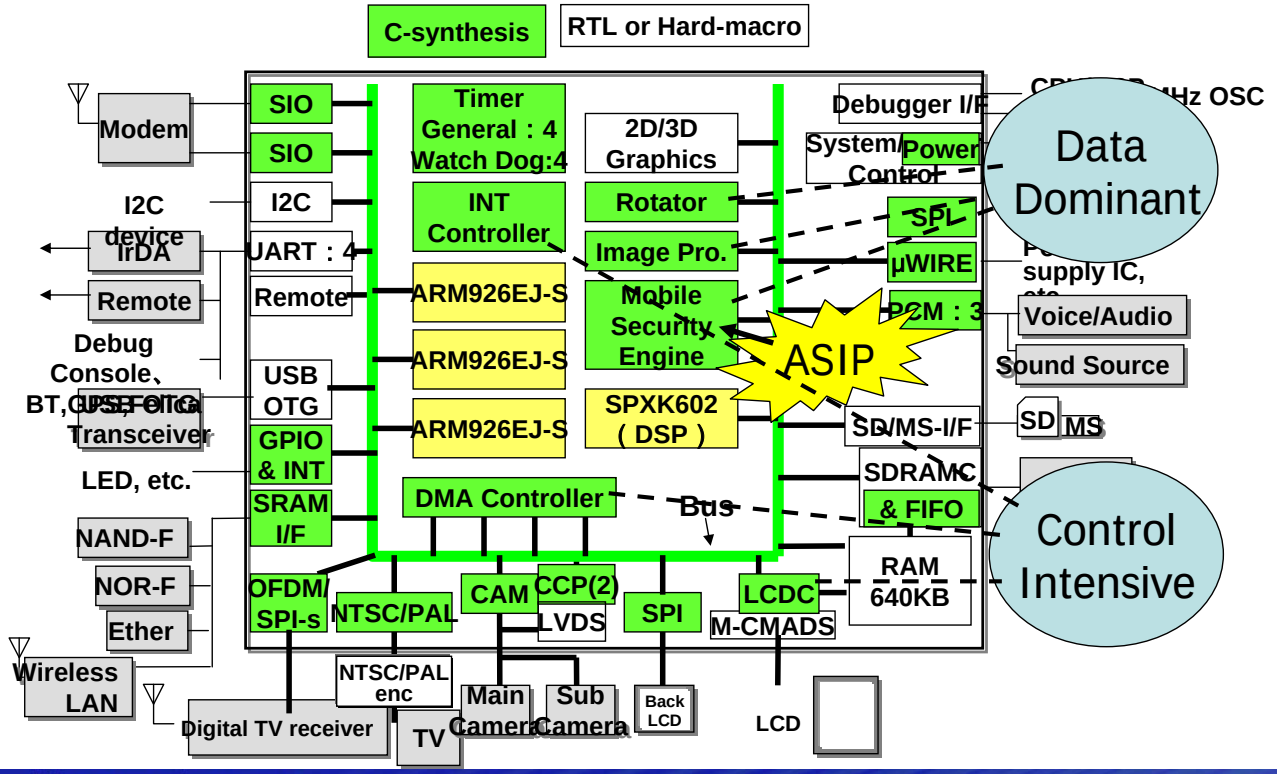
0) our Chip Architecture (MP-SoC)



looks typical, but has some interesting features

Various modules are behaviorally synthesized from C!

3G Mobile Phone Application Chip (MP211:ISSCC05)



1) Reconfigurable Hardware:

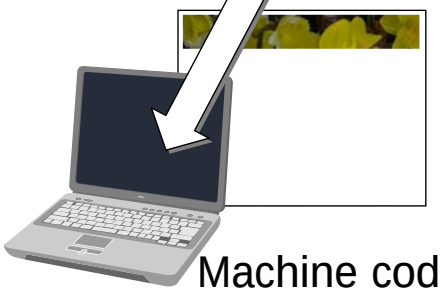
*C-synthesis + **Dynamic Reconfigurable Processor***

Ex1: graphic

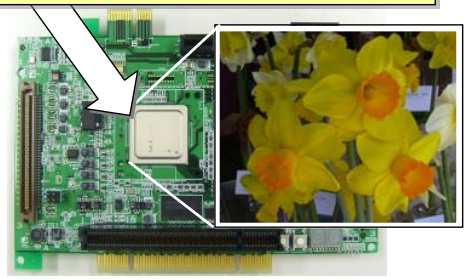
Image Processing Algorithm, **in C**

Gnu C Compiler

Behavioral Synthesizer



Machine code



Configuration code

Pentium Core2

Reconfigurable HW

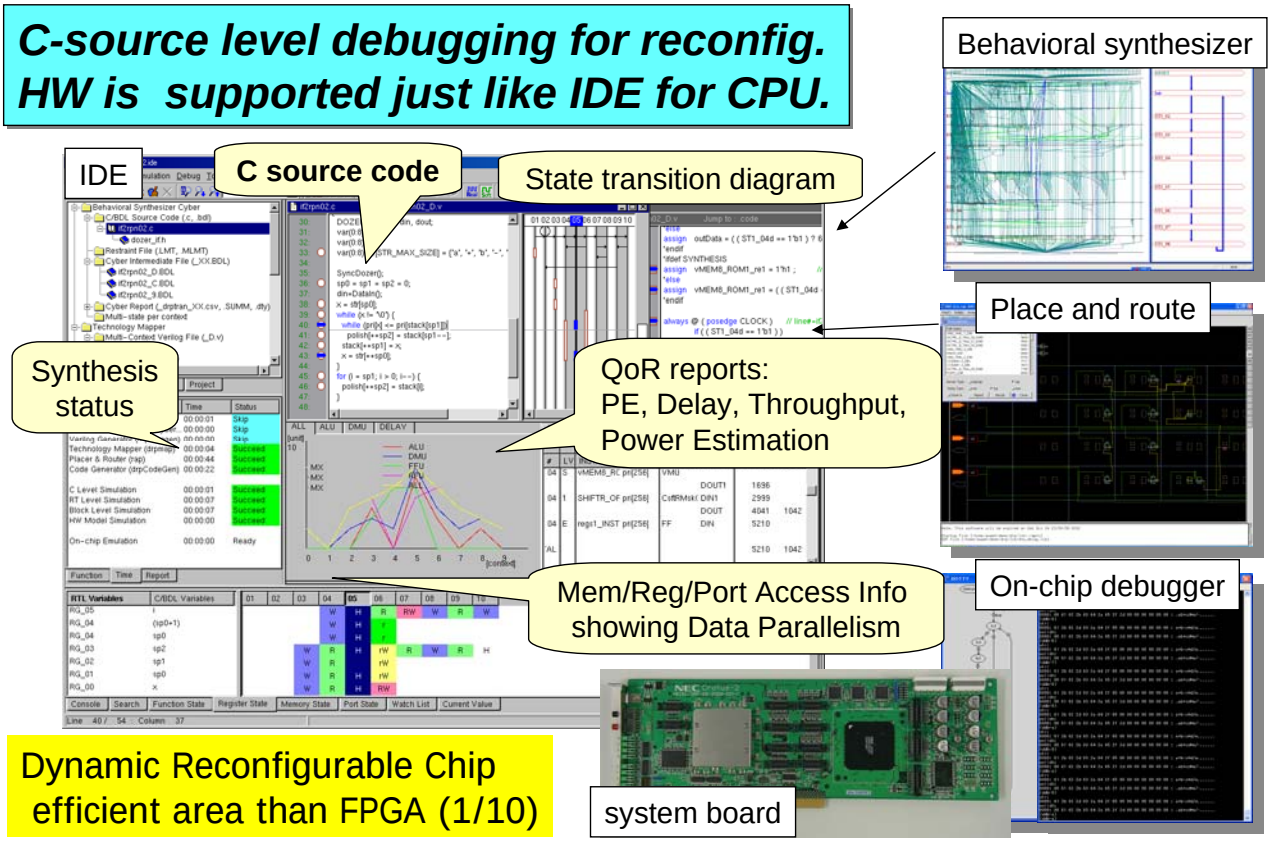
@ 1.8 GHz (1)
2,670ms/pic(1)

Performance: 20x with 1/40 freq.

@50MHz (1/40)
110ms/pic(20x)

Fully Integrated Design Environment

C-source level debugging for reconfig. HW is supported just like IDE for CPU.

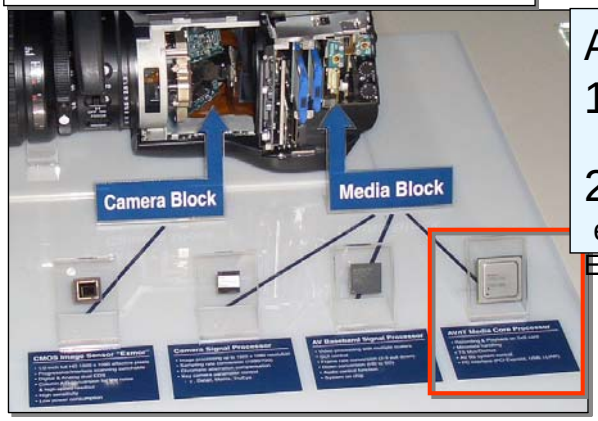


Dynamic Reconfigurable Chip
efficient area than FPGA (1/10)

C-synthesis + Reconfigurable Hardware

Ex2. High Speed HD video Professional Camcorder

AV/IT Media Core Processor



After chip fabrication (in a system)

1) spec could be **modified**
   e.g. TS Packet Mux/DeMux
2) new functions can be added
   e.g DMA.MP2 Audio Encoder、DV Encoder/Converter

Keys:
- Dynamic reloading
- Programmability from C like CPU (RTL design never work)

Effects:

- Avoid chip rework (chip modifiable in system)
- Keep deadline of system delivery
- ***Reuse the chip to another equipment***

Dynamic Reconfigurable Processor roll in ASSP

1)Programmable HW (faster than DSP, GPU)
HW performance

2) Proxy of embedded CPU
embedded CPU is not so powerful enough to perform multiple tasks.
-> Several embedded software are employed on our programmable HW (controller, processing)

Techniques:
Dynamic configuration Reloading (task switching)
can handle several different tasks

DRP gives flexibility to ASSP, ASIC
(CPU does not have enough performance)

2) Analysis on C-synthesized HW modules
QoR: Behavioral Synthesis vs Manual RTL

ex1)Fixed Architecture (e.g. Processor):

Configurable processor	C(HLS)	RTL(Man.)	Ratio
#lines	1.3KL	9.2KL	7.6X
Sim. speed	61Kc/s	0.3K cycles/sec	203X
Size	19KG	18KG	5%+

Not much space for architectural exploration
HLS cannot beaten good designers, but
7times less code size, and
200X faster simulation lead to
less bugs, less design period

QoR analysis (cnt.)

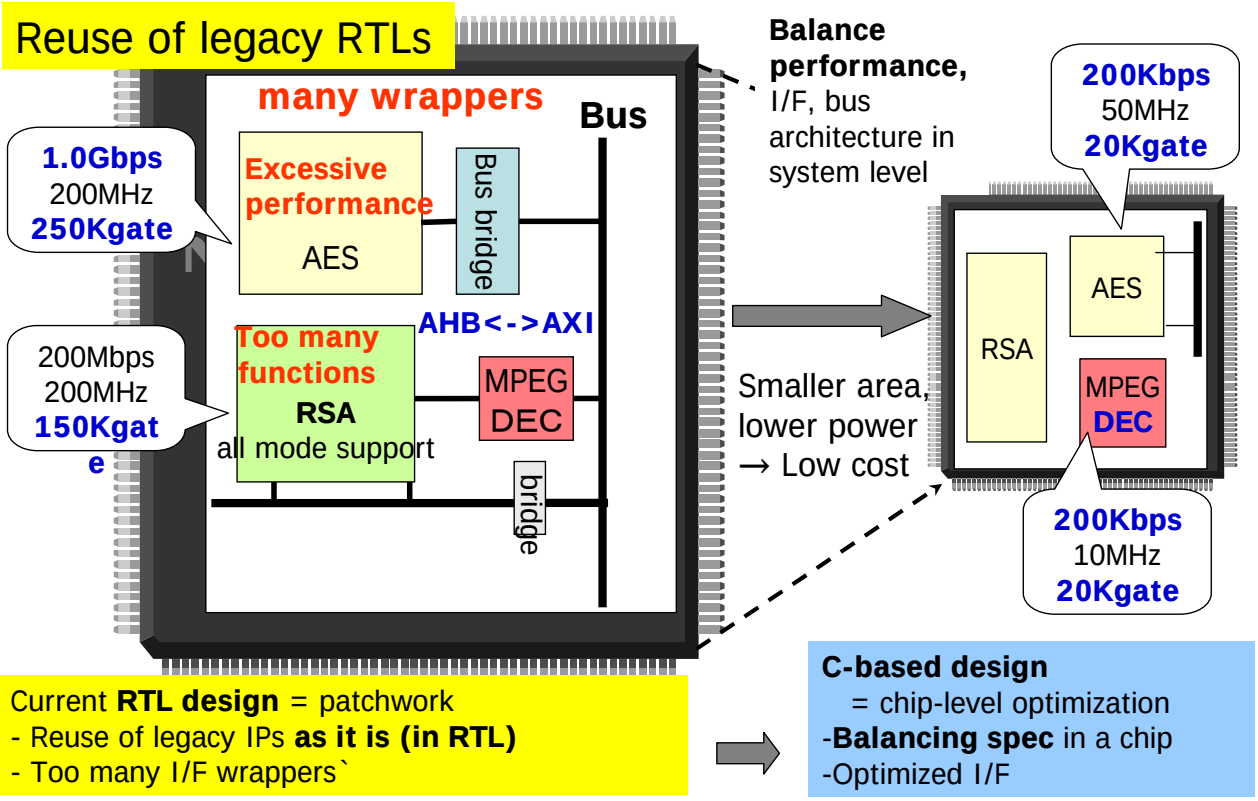
ex2) Low Performance for **sequential algorithm**
(ex. ECC for Mobile Phone)

Constraint length: 9, Data rate: 1/2, word 8bit, ACB 4 parallel
Decode: Cycles 10,882 clocks , speed 0.68ms (at 16MHz clock)

Viterbi decoder	C(HLS)	RTL(Man.)	Ratio
Size	5 KG	50 KG	1/10

-Human Designer is good at high performance design
usually, fully parallel architecture
-HLS is good at time multiplexed architecture
-> sharing REGs and FUs -> smaller circuits.

C-based Design Enables Chip-level Optimization



QoR (cnt.)

ex3) **High Performance** Circuit (highly parallel or pipelined)

- High speed RSA-2048 circuit
  - Conventional implementation … 5-10 ms@100MHz

	C-synthesis	Hand-made RTL	Ratio
Latency (encryption)	**1 ms @100 MHz**	**1 ms @100 MHz**	**-**
Circuit size	**75 Kgates**	**60 Kgates**	**1.2**
Code size	**1000 lines**	**2000 lines**	**2x**
Simulation time (encryption)	**2 sec (behavioral sim.)**	**11min (680 sec) (RTL sim.)**	**300x**
After C modeling	2 minutes	3+ days	

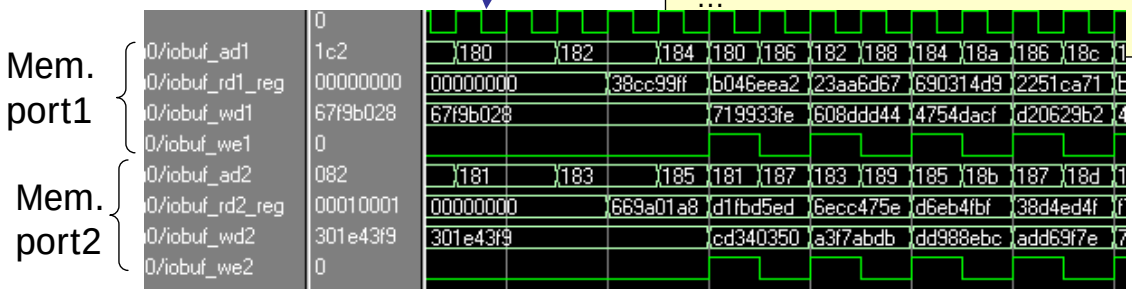
Merits of using behavioral synthesis

Some Area Penalty still remains, but ….

- Readable source code, high maintainability
- **No cycle-timing errors**
  - Easier debugging
  - Reduce # of corner test cases
  - Higher LSI reliability

Automatic Timing Optimization
- Continuous memory access
- Full use of **multi-ports of Mem.**
- **Pipelined** multipliers

```
void Montgomery_mult(…)
{
  …
  /* Cyber FOLDING = 2 */
  for (idx_y = 1; idx_y < blklen; idx_y++) {
    acc   =   acc(95, 32)
            + x_ini * MEM[y + idx_y];
            + en * MEM[m + idx_y];
            + MEM[s + idx_y];
    MEM[s + idx_y – 1] = acc(31, 0);
  }
  …
```



Summary

1) C-synthesis + DRP leads to **Flexible LSI** (HW)
 - Fully C programmable HW for control dominated and data dominate circuits.

2) C-synthesized HW
 good for system level optimization
 (balancing performance of each functional IPs)

3)Other topics for success
 - C source level verification (source code debug)
 - formal veri. (equiv. prove & property checking)
 - test bench gen. (guided random patterns)
 - ECO, Timing Closure, ...

Thank you!

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